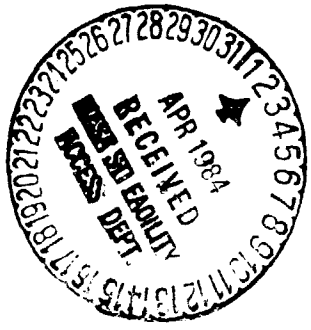
TECHNICAL MEMORANDUM (NASA) 90

PROCESSOR-CONTROLLED TIMING MODULE FOR LORAN-C RECEIVER

Hardware documentation is provided for the modified Loran-C timing module, which uses direct software control in determining loop sample times. Computer loading is reduced by eliminating polled operation of the timing loop.



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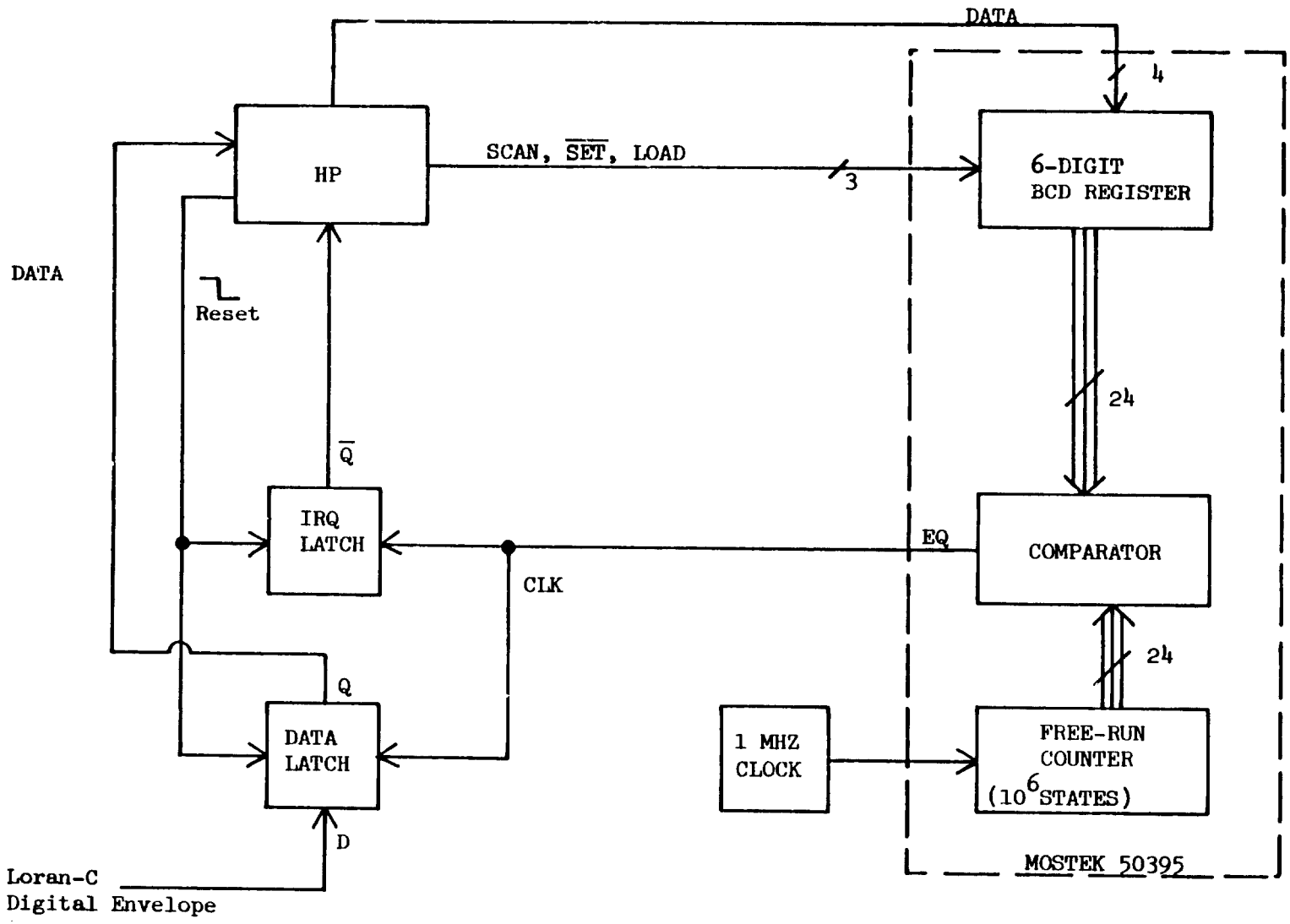


Figure 1. Block Diagram, Loran-C Timing Module.

II. CIRCUIT DESCRIPTION

Figure 2 shows the complete logic diagram for the Loran-C timing module. To the far left are signal descriptors for the system computer, an MAI SuperJolt based upon the MOS Technology 6502 with 6520 peripheral interface adapter (PIA). All connections, except for CLOCK and IRQ, are made through the 6520 PIA. Figure 3 gives a summary of PIA pin assignments, useful in software design and coding. The Mostek 50395 chip description is given as figure 4, and pinouts are shown in figure 5.

Referring to figure 2, note that seven lines provide data and control signals to the Mostek IC (U3). All these signals are output by the computer as TTL-compatible signals, and must be changed to the 12-volt MOS specification required by U3. This conversion is performed in open-collector drivers U1 and U2, pulled up to 12v through 1.1 K-ohm resistors. These lines carry the four data bits for register digits Ra, Rb, Rc and Rd, the LR (Load Register) strobe and $\overline{\text{SET}}$ (Set digit counter to most-significant digit) signals.

The timing chip U3 is wired for free-running counter, counting up, and is driven by the CLOCK, which is a buffered version of the main microcomputer clock (a temperature-compensated crystal oscillator). The SCAN input which increments the digit counter to indicate the load window for each register digit is driven by the computer via the SCAN line.

The computer is programmed to select ($\overline{\text{SET}}$) the high order digit first, and to set LR to enable the register load digit at a time. Each digit is then placed on RA through RD, and loaded by toggling SCAN.

Once the register is fully loaded, the U5 Loran-C interrupt and data latches are enabled by bringing $\overline{\text{CLRP}}$ high. When the free running counter in U3 reaches the register value just loaded, U3 issues an EQUAL pulse for one clock period (one μs) which clocks the U5 latches. The IRQ low since the $\overline{\text{Q}}$ output of the U5 interrupt latch always goes low upon clocking. An interrupt is signaled at $\overline{\text{IRQ}}$ to the computer. LDAT, latched by the U5 Loran-C latch, assumes the instantaneous value of the Loran-C digital waveform received at $\overline{\text{LRIN}}$ from the receiver front-end module. Note that $\overline{\text{LRIN}}$ is processed by U4 to set a pulse width of approximately 70 μs before it is sampled. This pulse width is necessary to provide a guard time after the leading pulse edge to permit successful pulse tracking, and to minimize initial search time. Since the various front-end processors designed to date have presented various pulse widths, this U4 mono-stable multivibrator has been provided to equalize the waveform before sampling.

The remainder of the circuit, U12, deals with receiver features included for evaluation. The event latch is driven by a front-panel pushbutton to place on the receiver output tape a unique mark so output data may be correlated with flight events. The retrack latch, also operated by pushbutton, signals the computer that the operator wishes to restart the Loran-C search process. To minimize contact bounce, these latches are configured to operate on the pushbutton release cycle.

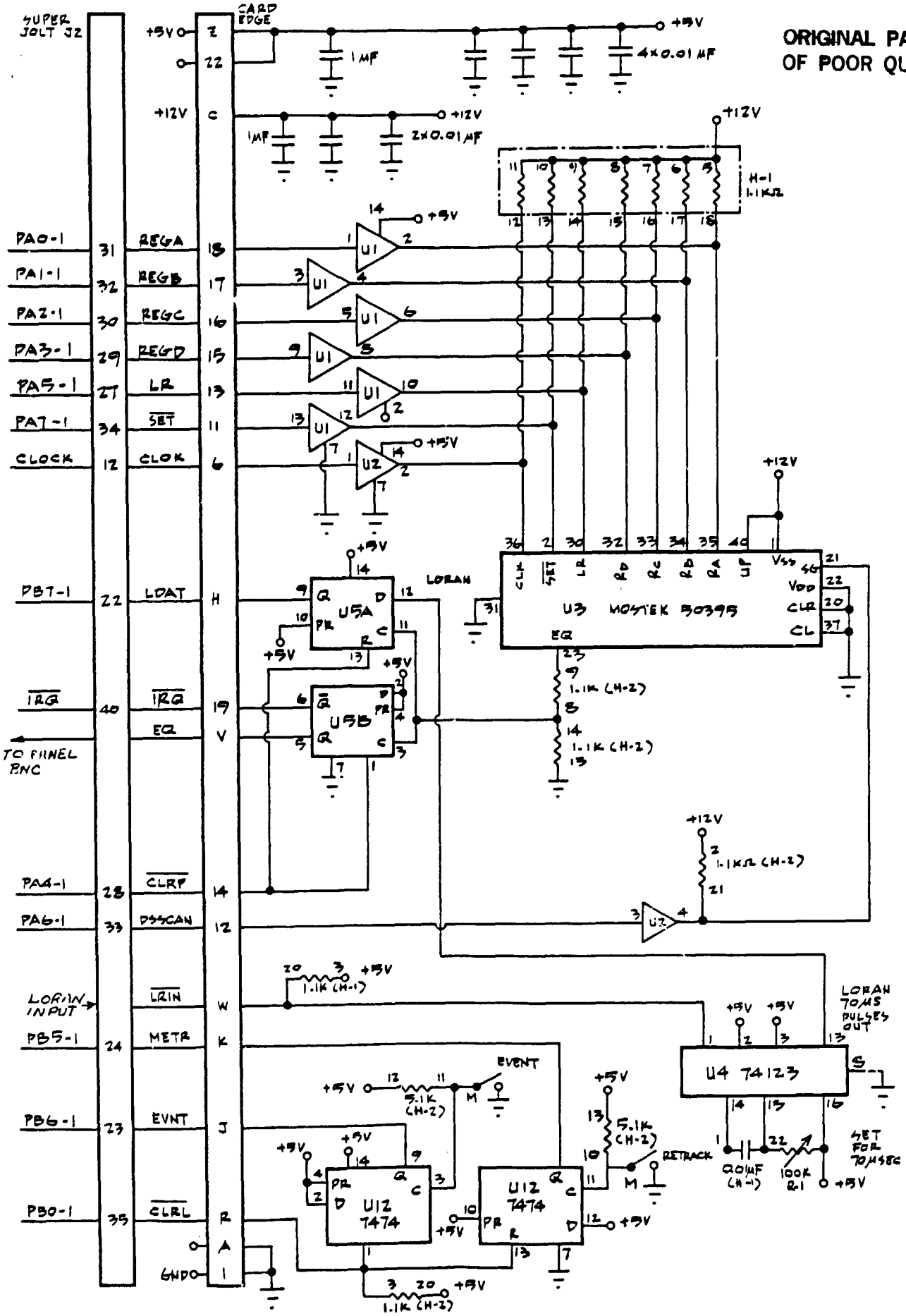


Figure 2. Revised Timing Board Schematic

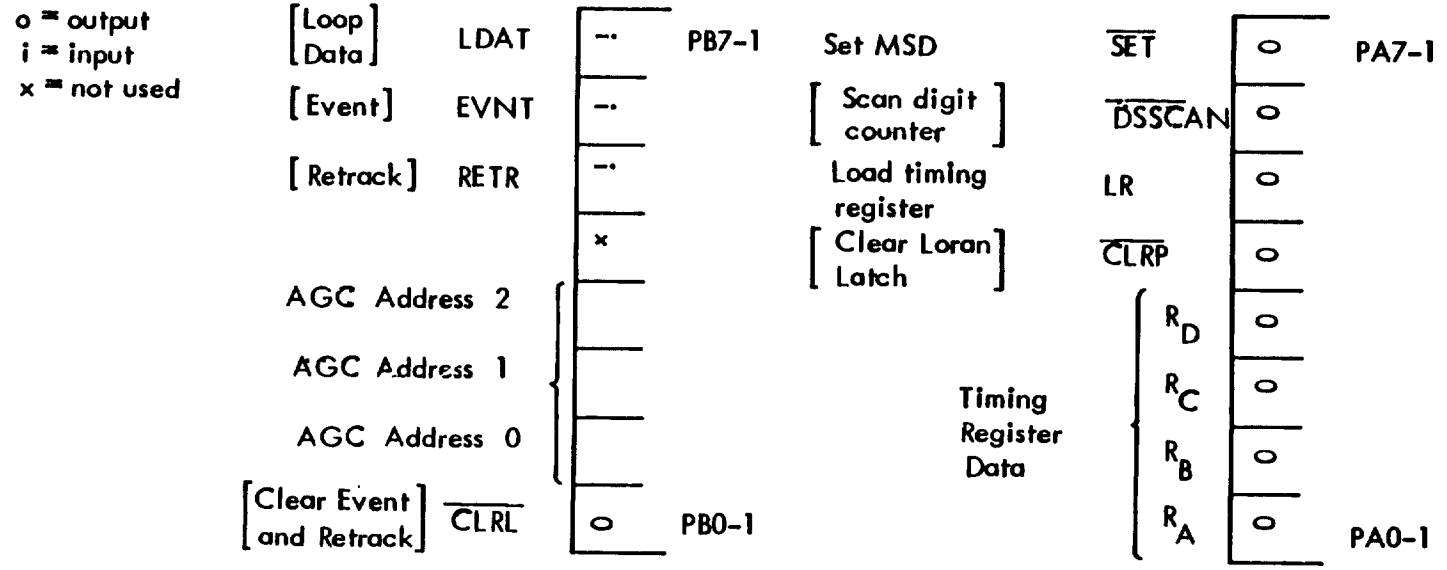


Figure 3. Super Jolt To Timing Board Summary of PIA Assignments

FUNCTIONAL DIAGRAM

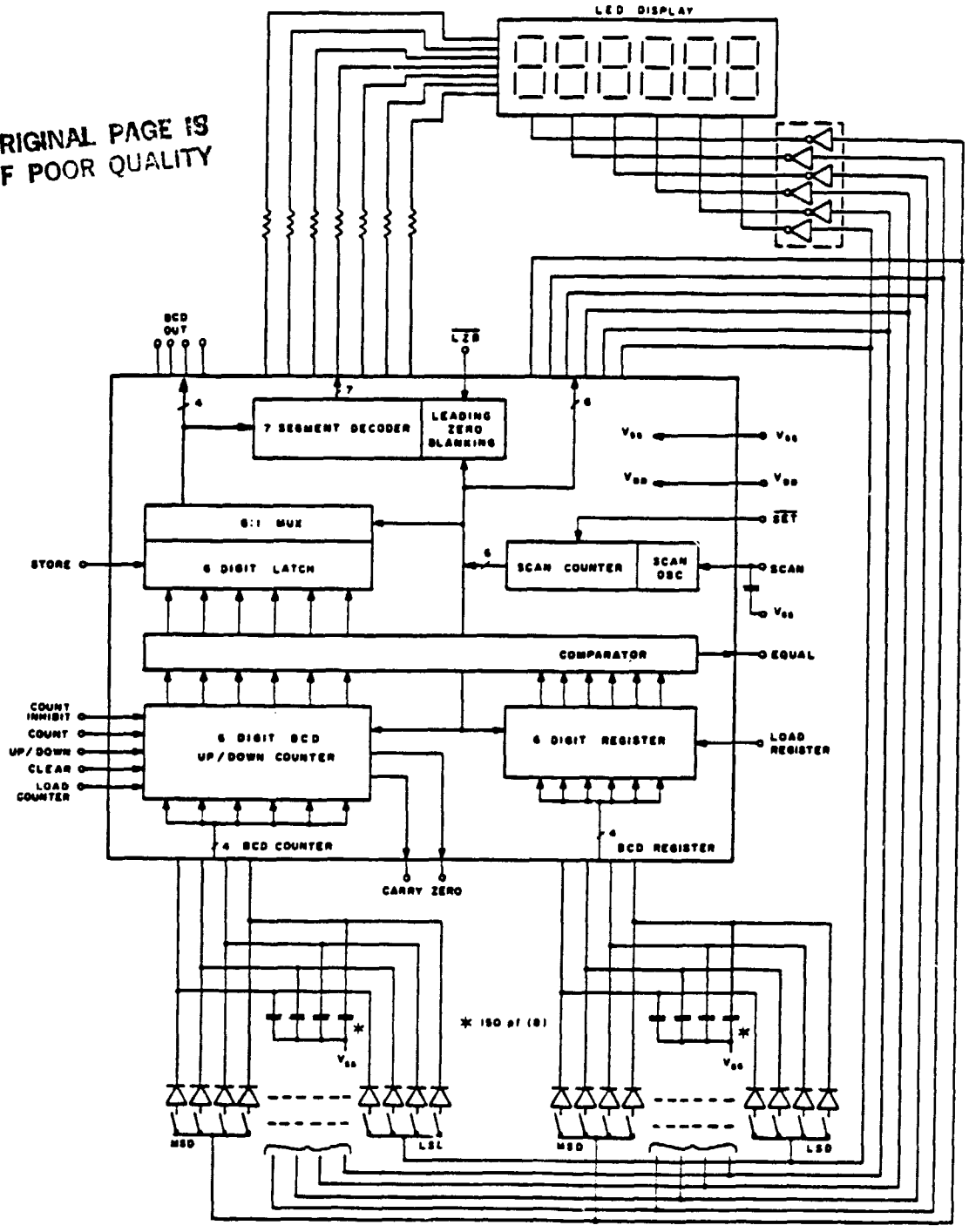


Figure 4. MOSTEK 50395 Integrated Circuit

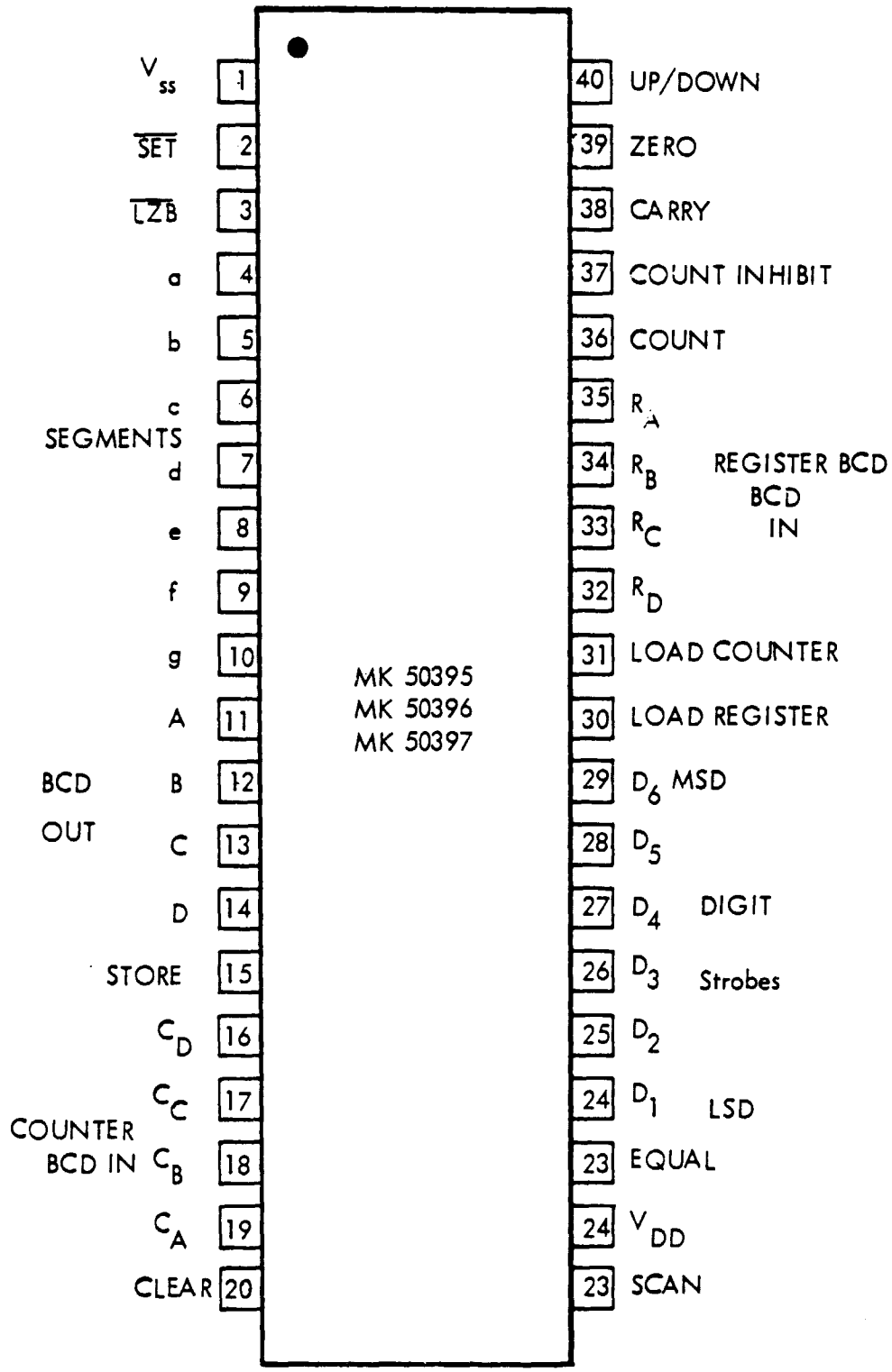
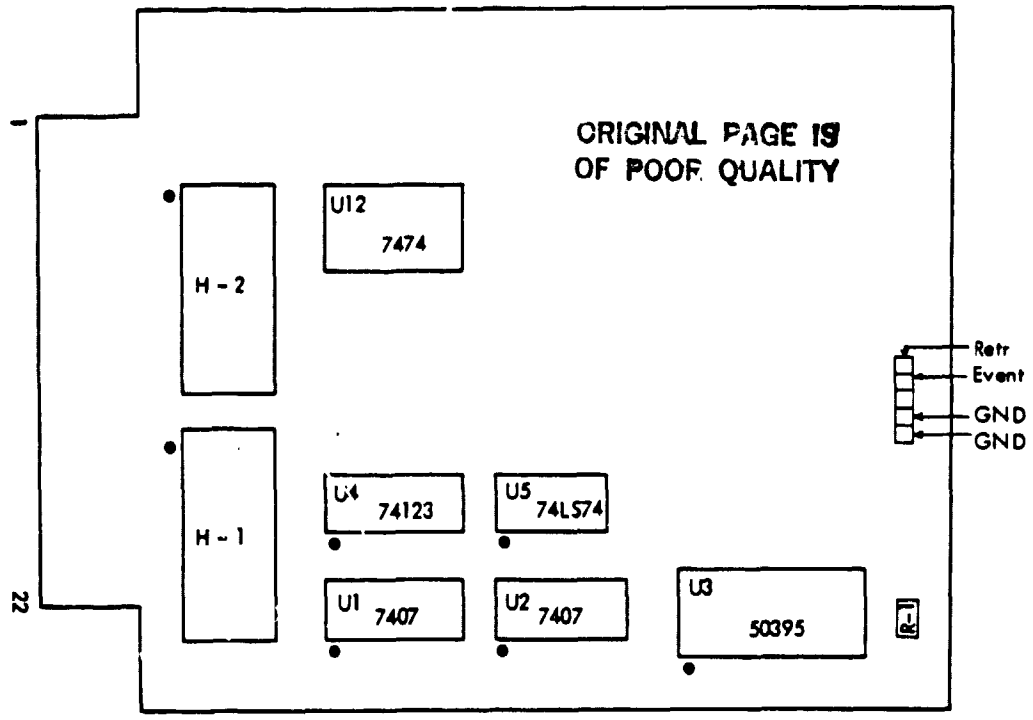


Figure 5. MOSTEK 50395 Pinouts

Once the computer program has serviced the Loran-C sample interrupt thus generated, the U5 latches are disabled by a low at $\overline{CLRP}$. Another register load sequence begins.

In this manner, successive samples may be taken of the Loran-C input waveform at times which are precisely controlled by the microcomputer. The programmer may now select algorithms for detecting received Loran-C chains and stations by varying the sample time and observing the result at LDAT.

The module pictorial appears in figure 6, giving placement of ICs and other major components.



Pin	Signal	Description
R	$\overline{\text{CLRL}}$	Low clears retrack & event latches.
J	EVNT	High indicates user event mark, cleared by $\overline{\text{CLRL}}$.
K	RETR	High indicates user retrack, cleared by $\overline{\text{CLRL}}$.
W	$\overline{\text{LRIN}}$	Input Loran-C pulses from front-end. TTL, open-collector, pulled up to 5V on this board
18	REGA	4-bit BCD digit load for U3 register.
17	REGB	
16	REGC	
15	REGD	
13	LR	Load 50395 (U3) Register strobe.
11	$\overline{\text{SET}}$	Set U3 to MSD for data load.
6	CLOK	1 MHz clock, from microcomputer.
12	DSSCAN	Scan Input for Digit Counter
14	$\overline{\text{CLRP}}$	Low clears Loran data latch.
H	LDAT	Loran data - loop sample output.
19	$\overline{\text{IRQC}}$	Combined IRQ from loop and digit strobes.
V	EQ	Equal pulse, for monitoring.

Figure 6. Pictorial and Signal Glossary

III. REFERENCES

[1] Lilley, R. W. and D. L. McCall, "A Loran-C Prototype Navigation Receiver for General Aviation," paper (No. 81-2329), presented at the AIAA/IEE Fourth Digital Avionics Systems Conference, November 1981.

[2] Lilley, R. W. and D. L. McCall, "A Loran-C Prototype Navigation Receiver for General Aviation," (NASA) Technical Memorandum 80, Avionics Engineering Center, Department of Electrical and Computer Engineering, Ohio University, August 1981.